REMARKS

Various combinations of claims 1-28 stand rejected under 35 U.S.C. 112, second paragraph and/or 102(e). Claims 29-40 were withdrawn in view of a previous restriction requirement and have been cancelled in this amendment. Applicants have additionally cancelled claims 2, 10 and 18 and amended claims 1 and 12. Claims 1, 3-9, 11-17, 19-26 and 28 remain pending in the application. Reconsideration of the application is respectfully requested.

Rejections Under 35 U.S.C. 112

The Examiner rejected claims 3-6, 11, 14, 15, 19 and 20-28 under 35 U.S.C. 112, second paragraph. Turning initially to claim 3, the Examiner expressed some concern as to whether a semiconductor structure comprising an island surrounded by an insulating material is supported by the specification. Applicants respectfully direct the Examiner's attention to page 5, lines 19-24 wherein it is stated

> The insulator substrate 34 and the insulating film 36 subdivide the active regions 26, 28 and 30 into semiconductor islands. That is, the active regions 26, 28 and 30 are laterally and vertically electrically isolated by insulating material. An interconnect layer 38 is formed in the base substrate 32 to interconnect the Peltier devices 14, 16 and 18 to contact structures 40 and 42 which may be coupled to a voltage source as indicated by the plus and minus symbols.

The Examiner is also encouraged to refer back to FIG. 1 of Applicants' drawings and observe semiconductor structures 26, 28 and 30 which are surrounded by insulating material 36 so as to define islands.

Regarding claim 4, the Examiner also expressed hesitation regarding how the insulating material may comprise part of the insulating substrate. The Examiner is directed to page 9, lines 3-15. Therein, it is stated that "[o]ptionally, a reverse process may be used, that is, the insulator film 36 fabrication may precede the deposition and planarization of a semiconductor film from which the islands 26, 28 and 30 may be defined." In addition, the subject matter in claim 4 as originally filed constitutes part of the specification for support purposes. Taken together, the aforementioned portion of page 9 and subject matter of claim 4 as originally filed supports a claim directed to a device wherein the insulator film 36 is integral with the insulating substrate 34.

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Regarding claim 6, the Examiner has taken the position that it is "not clear how the heat slug is in the insulating film." Applicants assume that the Examiner is referring to the Peltier Effect heat transfer device instead of a heat slug.[1] For an exemplary embodiment incorporating a Peltier Effect heat transfer device positioned in an insulating film on an insulating substrate, the Examiner is directed to FIG. 1, which depicts an insulating film 34 positioned on a base substrate 32, which may be an insulator or a semiconductor as desired and a Peltier effect heat transfer device 18 which is positioned in the insulating film 34.

Regarding claim 11, the Examiner stated that it was unclear how the Peltier effect heat transfer device comprises p-n junctions. The Examiner is respectfully directed to the paragraph beginning on page 5, line 25 and carrying over to page, lines 1-6 for an explanation as to the subject matter of claim 11.

Regarding claims 14 and 22, the Examiner has taken the position that it is unclear how the insulating material comprises part of the insulating substrate. Again, the Examiner is referred to the responsive argument presented above relating to claim 4.

Regarding claims 15 and 23, the Examiner has taken the position that it is unclear how the insulating material comprises part of the insulating substrate. Again the Examiner is referred to either FIGS. 1 or 20 and the responsive argument set forth above relating to claim 4 as to a supporting basis for claims 15 and 23.

Regarding claim 20, the Examiner stated that there was a potential issue regarding the recitation of a plurality of circuit devices positioned on the semiconductor layer. Applicants direct the Examiner to page 4, lines 30-31 and carrying over to page 5, lines 1-6 in which three circuit devices 20, 22 and 24 are depicted on a semiconductor layer consisting of active regions 26, 28 and 30. The recitation of at least one Peltier effect heat transfer device merely means that the claim covers a device in which one or more of the semiconductor islands have a Peltier effect heat transfer device.

Regarding claims 11, 19 and 28, the Examiner additionally commented that "it is unclear as to exactly how p-n junctions are present in the Peltier slug." The origin of the term "slug" is

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[1]The phrase "heat slug" does not appear in the claims.

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unknown as that term does not appear in Applicants' specification or the principle reference cited against claims, namely, U.S. Patent No. 6,476,483 to Adler et al. However, an exemplary structure showing the multiple p-n junctions that make up the Peltier Effect heat transfer device is shown in FIG. 2 and described on page 5, lines 25-31 and again on page 6, lines 1-6.

Rejections Under 35 U.S.C. 102

The Examiner rejected claims 1-28 under 35 U.S.C. 102(e) as being anticipated by Adler et al. The Examiner has directed Applicants to FIG. 1C of Adler et al. and flipped the structure depicted therein upside down for the purposes of applying that structure to claims 1-28. With the structure depicted in FIG. 1C of Adler et al. flipped upside down, the Examiner has taken the position that the interlevel dielectric layer 38 composed of oxide is an insulating substrate and the active layer 16 (that is in reality positioned beneath the interlevel dielectric layer 38) is positioned on the interlevel dielectric layer 38.

Preliminarily Applicants contend that it is doubtful that the person of ordinary skill in the art would interpret an interlevel dielectric layer that is formed over active regions and used to provide lateral electrical isolation for conductor plugs 40 and 42 as constituting an insulating substrate. However, Applicants have amended claim 1 to incorporate therein the subject matter of claim 2. Claim 1 now recites, *inter alia*, that the Peltier effect heat transfer device is not in the semiconductor structure that is positioned on the insulating substrate. Claim 12 has been amended in like but not identical fashion. Claims 1 and 12 as amended distinguish not only over the embodiment disclosed in FIG. 1C but also the embodiment disclosed in FIG. 4C of Adler et al.[2]

Applicants now address a few features of the rejected claims more particularly. With regard to claim 4, Applicants submit that Adler et al. does not disclose a semiconductor structure comprising an island surrounded by an insulating material wherein the insulating material comprises part of the insulating substrate. This is so because the only means of fabricating the isolation volume 26 depicted in FIGS. 1C and 4C (albeit not numbered in 4C) is by selective

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[2]Of course, dependent claims 3-9, 11, 13-17 and 19 are similarly distinguishable as well.

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etching of the active silicon 16 and subsequent bulk fill of silicon dioxide. In other words, the isolation volume 26 is deposited as a separate layer on the oxide layer 14.

Regarding claim 11, Applicants submit that Adler et al. does not disclose a Peltier effect heat transfer device that comprises a plurality of p-n junctions connected in series. The heat transfer device in Adler et al. consists of two metal structures, for example 57 and 53, fabricated in a stack. This structure is not a p-n junction.

For reasons similar to those advanced above with regard to claim 4, Applicants submit that claim 14 further distinguishes over Adler et al.

Independent claim 20 distinguishes over Adler et al. since that patent does not disclose a plurality of circuit devices positioned on a semiconductor layer.

For the reasons advanced above with regard to the patentability of claims 3-9, Applicants respectfully submit that claims 21-28 distinguish over Adler et al.

Applicants take this opportunity to make one further comment regarding the statement by the Examiner regarding the alleged disclosure of Adler et al. In particular, the Examiner stated that "see that a MOS device is disclosed, and therefore p-n junctions connected in series are inherent (see region 17)".[3] Applicants agree that FIG. 1A of Adler et al. does disclose source/drain regions 30 and 32 adjacent to a centralized channel region 25. However, those junctions between the source/drain regions 30 and 32 and the channel 25 do not constitute part of the Peltier effect cooling device and therefor have no relevance to Applicants' claims.

Conclusion

For the extensive reasons advanced above, Applicants submit that claims 1, 3-9, 11-17, 19-26 and 28 are patentable and respectfully request that a Notice of Allowability issue in due course.

Corrections to the Drawings

The Examiner requested that Applicants submit corrected drawings to show an insulating film positioned on a substrate and a plurality of junctions series connected. As to the insulating

[3]See instant Office Action, page 5, fifth sub-paragraph.

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film, Applicants respectfully refer the Examiner to FIG. 1, which shows an insulating film 36 positioned on an insulating substrate 32 or 34 (or the combination of the two).[4] As to the plurality of junctions, Applicants refer the Examiner to FIG. 2, which shows a plurality of p-n junctions provided by series-connected p-type impurity regions 46 and 48 connected in series to respective n-type impurity regions 50 and 52. The series connections between the respective impurity regions 48 and 52, and 46 and 50 are provided by a combination of the interconnect layer 38 and interconnect structures 54 and 56.

Accordingly, Applicants request the requirement for new drawings pertaining to these issues be withdrawn.

Applicants filed a set of formal patent drawings on December 31, 2002. Applicants then filed a corrected formal drawing sheet, sheet 6 of 10, to include a correct recitation of the figure number for FIG. 11. Applicants have submitted herewith two corrected drawing sheets, sheets 1 of 10 and 10 of 10. Corrected sheet 1 of 10 changes present element number "30" to element number --36-- and includes element number --30-- for the active region beneath the circuit element 24. Corrected sheet 10 of 10 changes present element number "130" to element number --136--, present element number "134" to element number --132--, and includes element number --130-- for the active region beneath the circuit element 124.

Applicants wished to further point out a few changes to the Examiner made in the formal patent drawings filed on December 31, 2002. In particular, FIG. 13 was amended by changing the element number 86 to 85 and FIGS. 17 and 18 were changed to include cross hatching of the layer 82 adjacent to the lower right corners of the structures 96 and 98.

Amendment to the Specification

Applicants have amended the specification to change the element number "84" to --85--.

The Examiner requested an amendment to page 11, line 9. However, Applicants believe the change to drawing sheet 10 of 10 takes care of the Examiner's objection.

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[4]See Applicants' specification, page 5, lines 7-10.

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Miscellaneous

The Assistant Commissioner is authorized to charge any required fees or credit any overpayment to Deposit Account No. 01-0365, Order No. AMDI:103\HON.

Respectfully submitted,

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